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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/826,198	04/15/2004	Symon Brewer	21-014	9819

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EXAMINER	
WONG, LINDA	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 07/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/826,198	BREWER, SYMON	
	Examiner	Art Unit	
	Linda Wong	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/20/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments, see Applicant's Remarks, filed 6/20/2006, with respect to the rejection(s) of claim(s) 1-20 under Kelkar et al (US Patent No.: 5663991) in view of Yanagisawa et al (US Patent No.: 6528982) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Behrin (US Patent No.: 5761254).

Response to Amendment

2. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Drawings

3. Applicant's arguments regarding the drawings filed 6/20/2006 have been fully considered but they are not persuasive. The applicant argues the examiner has "not provided a single reason why labels are necessary or essential, which is the explicit standard set forth in the Rules." The examiner respectfully disagrees. As stated below, the examiner has provided reasons as stated in the previously mailed office action as to why written descriptive labels are necessary and essential.
4. As stated previously, the drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. **Since the drawings have no written labels or worded descriptions have been**

provided in the drawings for any of the components, determination of what components or whether any of the components are shown cannot be performed. Therefore, all components must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

5. The examiner would also like to indicate to the applicant that such descriptive labels in the drawings would improve the quality of the application so one of ordinary skill in the art and examiners to determine the scope of the invention by viewing the drawings.

6. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and

informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

7. The applicant also remarked on the prosecution of a PCT case. The examiner would like to politely point out that the examiner is not privileged to discuss the prosecution of the PCT case in this US National Application. The examiner would like to point out that the current case in discussion is US Application No.: 10826198 and would like to politely indicate to the applicant's remarks regarding another case, specifically the PCT case remarked on in the Applicant's Remarks, should be discussed with the examiner during the prosecution of the PCT case and such remarks should be eliminated from discussion within the prosecution of this US Application, No.: 10826198. As a result, the examiner is not including a rebuttal regarding the comments referring to the PCT case as remarked upon in the Applicant's Remarks.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. **Claims 1-15** are rejected under 35 U.S.C. 102(b) as being anticipated by Guo (US Patent No.: 5400370).

   a. **Claims 1,6**, Guo discloses

      - using a tapped delay line (Fig. 1a, labels ruler delay and 22-23) for outputting data signal transition locations (Fig. 1a, labels 25-29),

- an edge distribution sampler (Fig. 1a, label 81) to latch the data signal transition location (Fig. 3, labels 810),
- converting the data transition location (Fig. 3, labels 25-29) to a delay value (Fig. 3, labels 831,835,836,833,834),
- converting the delay value to an edge position output (Fig. 3, labels 841,842 and B-S), and
- detecting a value of the edge position output (Fig. 3, label 82).

b. **Claim 11,** Guo discloses

- tapped delay line (Fig. 1a, labels ruler delay and 22-23) which delays the data signal SERIN, Fig. 1a, label 13, which produces delayed transition locations of the data signal (Fig. 1a, labels 25-29),
- sampling clock signal (Fig. 1a, label 16') or the "phase adjusted signal SBITCK 16' is used to strobe the sampler for capturing the status of the transitions" (Col. 6, lines 51-53),
- a sample register (Fig. 1a, label 81 or edge distribution sampler) or "edge distribution sampler 81 samples the level status of nodes 25 through 29 to capture the location of data transitions while the data signal wave is traveling in time ruler delays." (Col. 6, lines 45-49), wherein in the edge distribution sampler (Fig. 1a, label 81), the sampler latches the data signal transition location (Fig. 3, labels 810, 25-29),
- a priority encoder (Fig. 1a, label 82) or phase adjust decision receives the transition locations, which are detected from the sampler (Fig. 1a, labels 81

and 85), and uses the transition locations to determine up and down signals or delay value or the amount of adjustment or phase error (Col. 6, lines 66-67, Col. 7, lines 1-2 and Fig. 10, and Fig. 1a, labels 82,updnen,updn),

- a converter (Fig. 1a, label digital phase shifter or 56) or digital phase shifter uses the phase error or up/down signals produced by the phase adjust decision (Fig. 1a, label 82) for adjusting the digitally adjustable delay (Fig. 1b, label 60 and 50) with a delay value or amount of shift necessary or amount of delay (Fig. 1b, label 68, Col. 18, lines 61-67, and Col.19, lines 1-6), a converter (Fig. 1b, label 50) or digitally adjustable delay for adjusting the BITCK to output SBITCK, which is used as a sampling bit rate (Col. 6, lines 40-13, lines 20-24) and an edge position output since SBITCK is used as a signal for matching the delayed signals from ruler delay (Fig. 1a, label ruler delay) (Col. 6, lines 54-57, Col. 8, lines 5-20, lines 31-47, Col. 9, lines 21-67, Col. 10, lines 11-33) and
- a peak to peak calculation are shown in Fig. 5-9 and Fig. 3, labels 831-836,841-842, wherein the value of the edge positions are detected. (Fig. 5-9a-e, Col. 10,11, Fig. 9a-e for diagrams of outputs from Fig. 3, labels 831-836 and 841-842).

c. **Claims 2,7,12**, Guo discloses "the edge averaging mechanism has inherently low pass filtering functionality, since phase adjust decision command is not generated based on phase error of an individual edge but rather on an averaged edge position or the average of the phase errors for many bits." The

scheme for determining the amount of phase error already performs low pass filtering, since Guo discloses "for example, if each digitally controlled adjustable phase shift step is very small (delay of a minimum delay unit), a pure combinational logic may just be enough to map the E-L, I-O test outputs condition as the inputs to phase adjust control outputs UPDNEN and UPDN. Since the amount of phase adjustment allowed for each step is small, regardless of the phase error magnitude detected, another type of low pass filtering is embedded in the scheme." Since the digitally controlled adjustable phase shift step is performed prior to peak to peak computation (Fig. 3, labels E-L, I-O), the filtering is performed prior to peak to peak.

d. **Claims 3,8,13**, Guo discloses a data recovery method and apparatus, wherein the received signal has noise due to transmission atmosphere (Abstract, Col. 1, lines 42-46, Col. 2, lines 40-42), thus a dither signal or a signal with noise is already under test prior to the signal under test or the next received signal.

e. **Claims 4,9,14**, Guo discloses over-range detector for analyzing when the edge position movement or the peak to peak value or the output from the E-L test exceeds an absolute threshold number d. (Col. 11, lines 22-39)

f. **Claims 5,10,15**, Although Guo fails to disclose calculating the root mean square (RMS), Ishida et al discloses calculating the root mean square in a jitter measurer (Fig. 19, labels 107 and 108). It would be obvious to one skilled in the art to incorporate calculating the RMS to accurately estimate the amount of jitter in a signal so to eliminate for purpose of recovering data by providing "a

variance of the instantaneous waveform data to obtain its standard deviation". (Col. 9, lines 51-58)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. **Claims 16-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Guo (US Patent No.: 5400370) in view of IEEE Design and Test of Computers, "FPGA and CPLD Architectures: A Tutorial".

   a. **Claim 16** inherits all the limitations of claims 1,6,11, but claim 11 does not recite the limitation of a field programmable gate array carry chain (FPGA). Although Guo does no discloses an FPGA, based on the tutorial provided by IEEE Design and Test of Computers, "FPGA and CPLD Architectures: A Tutorial", an FPGA is a programmable array of flip-flops or logic gates. Guo discloses a variable delay line, which is equivalent to an FPGA. (Fig. 1a, label ruler delay) It would be obvious to one skilled in the art to provide an FPGA carry chain comprised of a interchanging or programmable delay line to provide a more robust, dynamic array of logics to decrease cost and provide very high pin-to-

pin speed performance. (Definitions: page 43 under Terminology, pg 43, Col. 3, line 4 and pg 44, Col. 1, lines 1-2)

b. **Claim 17** inherits all the limitations of claims 2,7,12.

c. **Claim 18** inherits all the limitations of claims 3,8,13.

d. **Claim 19** inherits all the limitations of claims 4,9,14.

e. **Claim 20** inherits all the limitations of claims 5,10,20.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Behrin (US Patent No.: 5761254)

b. Tabatabaei et al (US Patent No.: 6754613)

c. Yamaguchi et al (US Publication No.: 20030125888)

d. Soma et al (US Patent No.: 6795496)

e. Yamaguchi et al (US Publication No.: 20040062301).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linda Wong whose telephone number is 571-272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Cheih Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Linda Wong

/Kevin Kim/

KEVIN KIM
PATENT EXAMINER